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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,905	03/26/2004	Haowen Bu	TI-36637	9390

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TEXAS INSTRUMENTS INCORPORATED  
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DALLAS, TX 75265

EXAMINER
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STARK, JARRETT J

ART UNIT	PAPER NUMBER
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2823

NOTIFICATION DATE	DELIVERY MODE
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08/08/2007

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	Application No. 10/810,905	Applicant(s) BU ET AL.	
	Examiner Jarrett J. Stark	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 28 June 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) 11-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1, 5-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo (US 6,878,583 B2) and in view of Takenouchi et al. (US 5,061,649).

**Regarding claim 1**, Guo discloses a method for fabricating a CMOS transistor structure, comprising the steps of:

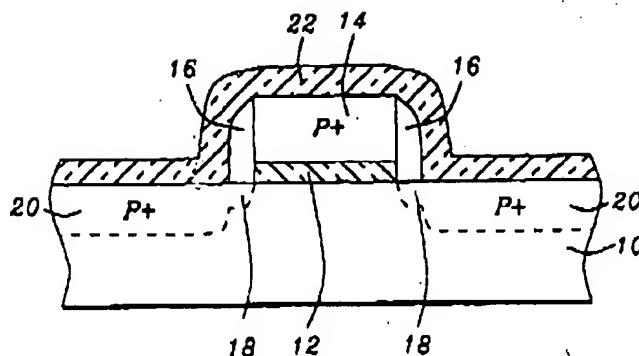


FIG. 4

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor and an N-type dopant region to support a P-channel transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure (Fig. 4 and Abstract);

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack (Fig. 4 #18);

forming a layer of insulating material over the lightly-doped extension regions Fig. 4 #16);

forming an interfacial layer of nitrogen at the interface of the insulating layer and the lightly-doped extension regions (the gate dielectric 12 and spacers 16 can be silicon nitride, thus Fig. 4 above will inherently have Nitrogen at the interface between the insulating material and the LLD.)

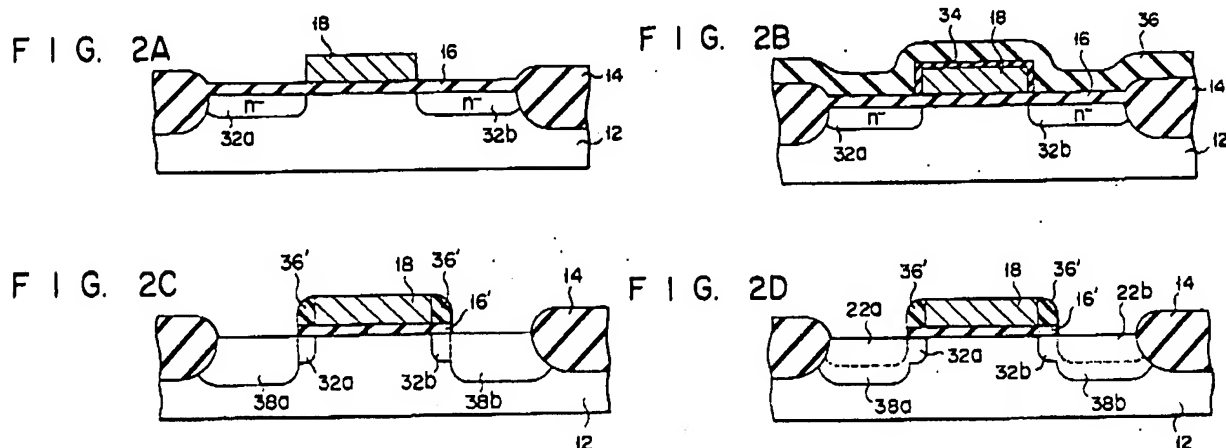
forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks (Fig. 4 #20);

forming a capping layer of contiguous silicon nitride over the semiconductor substrate and each of the gate stacks (Fig. 4 #22);

annealing, with the capping layer in place, the extension and source and drain regions; and

removing the capping layer after the annealing (Abstract-cap is removed where desired.)

Guo does not specifically disclose "forming a layer of insulating material over the total exposed surface of the lightly-doped extension regions. Guo discloses that the insulating layer is formed prior to forming the LDD region. It is however well understood and established in the art the LDD regions can be formed before or after the insulation layer is formed. An example of this is disclosed by Takenough et al. in figures 2A-2D.



It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Guo and Takenough to enable the LDD

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formation step of Guo to be performed according to the teachings of Takenouchi because one of ordinary skill in the art would have been motivated to look to alternative suitable methods of performing the disclosed LDD formation step of Guo and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

**Regarding claim 5,** Guo discloses the method of claim 1 wherein the insulting layer is selected from the group comprising silicon nitride and silicon oxide (Guo, claim 2).

**Regarding claim 6,** Guo in view of Takenouchi discloses the method of claim 1 wherein the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an  $\text{NH}_{3.3}$  thermal annealing, an  $\text{NH}_{3.3}$  or  $\text{N}_{2.2}$  plasma treatment, or an N implantation (Guo, claim 4).

**Regarding claim 7,** Guo in view of Takenouchi discloses the method of claim 1 wherein the capping layer has a thickness in the range of 200-1000 angstroms (Guo, claim 31).

**Regarding claim 8,** Guo in view of Takenouchi discloses method of claim 1 wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds (Guo, claim 22).

**Claims 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Guo in view of Takenouchi as applied to the claims above, and in further view of Moore (US 2003/0068855 A1).

**Regarding claim 9,** Guo in view of Takenouchi discloses the method of claim 1, however does not explicitly disclose wherein said gate stack further includes a nitride sidewall deposited with a BTBAS precursor. Moore discloses at the time of the invention it was known in the art to form silicon nitride layers and spacers with a BTBAS precursure (Moore, Abstract).

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Guo and Moore to enable the deposition step of Guo to be performed according to the teachings of Moore because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed deposition step of Guo and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

**Claims 2,3,4, and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo in view of Takenouchi in view of Tseng et al. (US 5,726,087), and in view of the following comments.

**Regarding claim 10**, Guo discloses a method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having an N-type dopant region to support an PMOS transistor and a P-type dopant region to support a NMOS transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure (Fig. 4 and Abstract);

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack (Fig. 4);

the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about  $1-2 \times 10^{20}$  atoms/cm<sup>3</sup> (Fig. 4,- see below regarding claims 2-4);

forming a layer of silicon oxide over the total exposed surface of the lightly-doped extension regions(Fig. 4).

the interfacial layer of nitrogen having an atomic nitrogen concentration in the range of 2-15 atomic percent (Fig. 4,- see below regarding claims 2-4);

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks (Fig. 4)



the source and drain regions in the in the N-type dopant region comprising a P-type dopant having a concentration in the range of about  $1-2 \times 10^{20}$  atoms/cm<sup>3</sup> (Fig. 4 and Abstract,- also see below regarding claims 2-4);

forming a capping layer of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms over the semiconductor substrate and each of the gate stacks (Fig. 4,- see below regarding claims 2-4);

annealing, with the capping layer in place, the extension and source and drain regions at a temperature in the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds; and removing the nitride cap after the annealing (Guo, claim 22).

Guo does not explicitly disclose forming an interfacial layer of nitrogen between the lightly-doped extension regions and the silicon oxide layer. As disclosed by Tseng it was known to form multilayerd gate dielectrics that include a oxide layer (Fig 12. layer 14) formed on nitrogen -containing thin interfacial layer (Fig 12. layer 13) on a base layer.

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Guo and Tseng to enable the gate dielectric formation step of Guo to be performed according to the teachings of Tseng because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed gate dielectric formation

step of Guo and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

**Regarding claims 2-4 and 10**, Guo in view of Takenouchi discloses the method of claim 1. The further recited limitations of specific dopant concentrations and specific atomic nitrogen concentration are merely structural limitations, which do not further limit a method claim. Structural Elements recited in the claim must manipulatively distinguish the claim from the prior art to have patentable weight.

"To be entitled to patentable weight in method claims, the recited structural limitations therein must affect the method in a manipulative sense and not amount to mere claiming of a use of a particular structure."

Ex parte Pfieffer, 135 USPQ 31,k 33 (Bd. Pat. App & Inter. 1961). Put another way, "patentability of a method claim must rest on the method steps recited, not on the structure used, unless that structure affects the method steps." Leesona Corp. v. U.S., 185 USPQ 156, 165 (Ct. Cl. Trial iv. 1975) aff'd 192 USPQ 672 (Ct. Cl 1976).

In Ex parte Pfieffer, 135 USPQ 31, 33 (Bd. Pat. App. & Inter. 1961) the clams set forth a method of dropping a rubber bag out of a airplane without the use of a parachute to transport free flowing material inside the bag to the ground. The applicant argued that the reference applied by the examiner did not use a rubber bag having walls of extremely high tensile strength capable of stretching several hundred percent and which was oblate in shape. The Board upheld the rejection based on the fact that the bag o the prior art is manipulated (filled, dropped, allowed to fall and a opened after impact) as

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claimed and that the structural differences of the bag do not alter these basic steps. In *Leeson Corp. v. U.S.*, 185 USPQ 156, 165 (Ct. Cl. Trial div. 1975) *aff'd* 192 USPQ 672 (Ct. Cl. 1976) the claim was directed to a method of recharging a battery having a gas permeable nonconsumable envelope cathode in which the spent anode was removed from the nonconsumable envelope cathode and replaced with a fresh anode. The court stated that, in this case, it is apparent that the claimed method steps are not affected by the claimed cathode structure since the very same method would be used with the box cathode of Heise." 185 USPQ at 165. The methods of recharging a battery "cannot be transformed into a patentably new one merely by using it to recharge a battery having cathode not shown in the prior art." *Id.* At 165 (emphasis added).

It is however noted that Guo does not specifically disclose the specific dopant concentration or a specific atomic nitrogen concentration.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the dopant and atomic nitrogen concentration through routine experimentation and optimization to obtain optimal or desired device performance because the dopant and atomic nitrogen concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation." Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jarrett J Stark  
Examiner  
Art Unit 2823

JJS  
July 30, 2007



MICHELLE ESTRADA  
PRIMARY EXAMINER